Institut de Recherche Interdisciplinaire de Grenoble

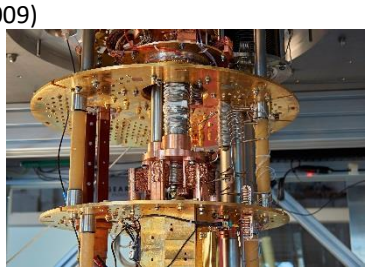
Pheliqs Quantum Physics & Engineering

Master / PhD Thesis Project

Superconducting Devices in Silicon

In the race towards building a quantum computer, even though the exact type of qubit that is the most suitable is not known, there is clearly a need for a large scale integration of quantum devices. As silicon technology is by far the most advanced technology, the possibility to fabricate quantum devices based on silicon will provide a serious and may be determinant asset to solid state qubits. The master internship that can be followed by a PhD thesis, focuses on the development and the study at very low temperature of CMOS compatible superconducting materials. The aim of the project is to fabricate superconducting silicon transistors where the source and drain are superconducting. Various materials can be envisaged such as silicides (PtSi, V3Si) and superconducting boron doped silicon (Si:B) obtained by laser annealing. At longer term, during the PhD, superconducting qubit based on gate tunable Josephson junctions will be investigated.
During the internship and PhD, the candidate will share his-her time between the LETI and the LaTEQS at IRIG/PHELIQS at the CEA Grenoble. At the LETI he-she will have access to the 200 and 300 mm facility to test structures and more elaborated devices that will be studied at very low temperature in the mK range using the experimental set-up's at LaTEQS.
This proposal is therefore at the frontier between state-of-the art technology and solid-state physics, applied technology and basic research, in the growing context of quantum technologies.
The candidate should have a strong interest for nanotechnology and experimental physics, together with a background in solid state physics.

F. Chiodi et al., *Proximity induced superconductivity in all silicon superconductor/normal junctions*, PRB 96, 024503, 2017
J.E. Duvauchelle et al., *Silicon Superconducting Quantum Interference Device*, APL 107, 072601 (2015)
T. Poiroux et al., *Highly performant FDSOI pMOSFETs with metallic source/drain,* Proceedings VLSI-TSA (2009)



Low temperature Cryostat at LaTEQS

Clean room facility at LETI

APPLY NOW!

To apply for this position, send your application (including CV) by e-mail to: francois.lefloch@cea.fr and fabrice.nemouchi@cea.fr

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